

IBM Docket # JP920000112 JS1

It is noted that on the cover sheet for the Final Office Action mailed February 4, 2003 the examiner rejected claims 1-3. However, in the body of the Office Action the Examiner rejected claims 1- 10 under 35 U.S.C. § 103(a) as being unpatentable over Ohnuma et al. in view of Gardner et al. '519. Applicants will respond to the current Office Action based upon the rejection of claims 1 - 10.

In response to the Examiner's rejection of claims 1 - 10 under 35 U.S.C. § 103(a) as being unpatentable over Ohnuma et al. in view of Gardner et al. '519, applicants traverse the rejection and believe that the claims are not made obvious by Ohnuma et al. in view of Gardner. Applicants' claimed invention requires "forming an oxide film on an inner wall of a CVD processing chamber" as part of the manufacturing method of an active matrix device including a top gate type TFT (see claim 1). Applicants' claimed invention further requires "a removable oxide film" being formed on "an inner wall of the processing chamber for forming the top gate type TFT" (see claim 11). Applicants' method claims further require a step process order of:

- forming an oxide film on an inner wall of a CVD processing chamber;
- arranging a substrate having source and drain electrodes formed therein in the processing chamber;
- doping the source and drain electrodes with P; and
- forming an a-Si layer and a gate insulating film in the processing chamber.

Applicants method claim 2 further require the step of removing the oxide film from the inner wall after the step of forming the a-Si layer and the gate insulating film.

Ohnuma fails to teach or suggest the "forming an oxide film on an inner wall of a CVD processing chamber" as part of the manufacturing method of an active matrix device including a top gate type TFT. Ohnuma further fails to teach or suggest "a removable oxide film" being formed on "an inner wall of the processing chamber for forming the top gate type TFT". Ohnuma still further fails to teach or suggest the order in which applicants' claimed method steps are presented. In particular, "forming an oxide on an inner wall of a CVD processing chamber" is performed prior to "doping the source and drain electrodes with p". This means preventing the dopant (phosphor) from being

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incorporated into the Si layer (6) during depositing the a-Si layer on a substrate soon after the step of doping **without the chamber changing.**

It is noted that the Examiner agrees with applicants points noted above. Namely, "Ohnuma fail to disclose forming an oxide film on an inner wall of a CVD processing chamber."

The Examiner then relies on Gardner for a teaching "forming an oxide on an inner wall of a CVD processing chamber" and cites column 6, lines 8 – 14. However, Gardner does not teach the forming of an oxide film on an inner wall of a CVD processing chamber. To the contrary, Gardner teaches away from the step of forming an oxide film on the wall of the chamber as an intended result of the process. The Examiner's attention is directed to column 6, lines 13 – 16 of Gardner. Gardner clearly teaches **"Cleaning of the chamber between runs reduces oxide build up on the showerhead and typically tends to increase oxide layer thickness uniformity between runs."** This teaches away from applicants claimed invention, namely forming an oxide film on the walls of the CVD chamber. Gardner teaches the forming of an oxide layer on a substrate. Specifically, Gardner states "A layer of oxide 403 is then formed over the substrate 401 using an oxide source showerhead as indicated at block 306" (See column 4, lines 54 – 55). Gardner does not teach or suggest applicants' claimed invention of forming an oxide on an inner wall as part of the process needed to make applicants' claimed invention. The mere fact that Gardner has to remove an oxide material from the inner walls (that was at best over spray for coating a substrate 401) of the chamber after the formation of a device does not lead one of ordinary skill in the art to make a device by forming an oxide film on the inner walls of a CVD chamber before applicants' device is made.

Therefore, Gardner et al. fails to solve the deficiencies of Ohnuma et al. Gardner et al. fails to teach or suggest the "forming an oxide film on an inner wall of a CVD processing chamber" as part of the manufacturing method of an active matrix device including a top gate type TFT. Gardner et al. further fails to teach or suggest "a removable oxide film"

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being formed on "an inner wall of the processing chamber for forming the top gate type TFT". Gardner et al still further fails to teach or suggest the order in which applicants' claimed method steps are presented. In particular, "forming an oxide on an inner wall of a CVD processing chamber" is performed prior to "doping the source and drain electrodes with p". Again, Gardner et al teaches away from applicants' claimed method by "removing any native oxide" before a layer is formed, see step 304 in Figure 3, column 4, lines 42 - 46 and column 3, lines 16 - 20. Accordingly, it is believed that Ohnuma et al cannot make obvious applicants' claimed invention, either singularly or in combination with Gardner et al under 35 U.S.C. § 103(a). Furthermore, there is no motivation or suggestions for one skilled in the art to combine the teachings of Ohnuma et al. and Gardner et al as defined in claims 1 - 16. Again, if one were to use the teachings of Gardner et al, one would remove the oxide from Ohnuma et al. However, since Ohnuma et al does not have an oxide film to remove, as claimed in applicants' claims, Gardner et al adds nothing to the Ohnuma et al reference.

In view of the remarks herein, the Examiner is respectfully requested to reconsider the above-identified application and allow the claims therein. If the Examiner wishes to discuss the application further or if additional information would be required, the undersigned will cooperate fully to assist in the prosecution of this application.

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In the event that this response does not result in allowance of all such claims, the undersigned respectfully requests a telephone interview at the Examiner's earliest convenience.

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Applicants request entry of this paper so as to place the file history of this patent application in better form for appeal.

Respectfully submitted,

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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Applicants:

Date: December 4, 2002

Tsujimura et al.

Group Art Unit: 2823

Serial No.: 09 81,643

Examiner: Coleman

Filed: May 15, 2001

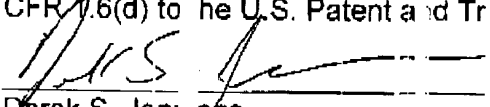
Docket No.: JP920000112US1

For: **METHOD AND APPARATUS FOR MANUFACTURING ACTIVE  
MATRIX DEVICE INCLUDING TOP GATE TYPE TFT**

Assistant Commissioner for Patents  
Washington, D.C. 20231

## CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper (1 pages) is being facsimile transmitted under Rule 37  
CFR 1.6(d) to the U.S. Patent and Trademark Office to (703) 872-9318 on April 4, 2003.

  
Derek S. Jennings  
Registered Patent Agent / Patent Engineer  
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RESPONSE TO THE OUTSTANDING OFFICE ACTION

## REMARKS

In response to the Final Office Action dated February 4, 2003, applicants offer the following remarks addressing the outstanding Final Office Action.

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It is noted that on the cover sheet for the Final Office Action mailed February 4, 2003 the examiner rejected claims 1-10. However, in the body of the Office Action the Examiner rejected claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over Ohnuma et al. in view of Gardner et al. '519. Applicants will respond to the current Office Action based upon the rejection of claims 1 - 10.

In response to the Examiner's rejection of claims 1 - 10 under 35 U.S.C. § 103(a) as being unpatentable over Ohnuma et al. in view of Gardner et al. '519, applicants traverse the rejection and believe that the claims are not made obvious by Ohnuma et al. in view of Gardner. Applicants' claimed invention requires "forming an oxide film on an inner wall of a CVD processing chamber" as part of the manufacturing method of an active matrix device including a top gate type TFT (see claim 1). Applicants' claimed invention further requires "a removable oxide film" being formed on "an inner wall of the processing chamber for forming the top gate type TFT" (see claim 11). Applicants' method claim further require a step process order of:

- forming an oxide film on an inner wall of a CVD processing chamber;
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Applicants method claim 2 further require the step of removing the oxide film from the inner wall after the step of forming the a-Si layer and the gate insulating film.

Ohnuma fails to teach or suggest the "forming an oxide film on an inner wall of a CVD processing chamber" as part of the manufacturing method of an active matrix device including a top gate type TFT. Ohnuma further fails to teach or suggest "a removable oxide film" being formed on "an inner wall of the processing chamber for forming the top gate type TFT". Ohnuma still further fails to teach or suggest the order in which applicants' claimed method steps are presented. In particularly, "forming an oxide on an inner wall of a CVD processing chamber" is performed prior to "doping the source and drain electrodes with p". This means preventing the dopant (phosphor) from being

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incorporated into the Si layer (6) during depositing the a-Si layer on a substrate soon after the step of doping **without the chamber changing.**

It is noted that the Examiner agrees with applicants points noted above. Namely, "Ohnuma fails to disclose forming an oxide film on an inner wall of a CVD processing chamber."

The Examiner then relies on Gardner for a teaching "forming an oxide on an inner wall of a CVD processing chamber" and cites column 6, lines 8 – 14. However, Gardner does not teach the forming of an oxide film on an inner wall of a CVD processing chamber. To the contrary, Gardner teaches away from the step of forming an oxide film on the wall of the chamber as an intended result of the process. The Examiner's attention is directed to column 3, lines 13 – 16 of Gardner. Gardner clearly teaches **"Cleaning of the chamber between runs reduces oxide build up on the showerhead and typically tends to increase oxide layer thickness uniformity between runs."** This teaches away from applicants claimed invention, namely forming an oxide film on the walls of the CVD chamber. Gardner teaches the forming of an oxide layer on a substrate. Specifically, Gardner states "A layer of oxide 403 is then formed over the substrate 401 using an oxide source showerhead as indicated at block 306" (See column 4, lines 54 – 55). Gardner does not teach or suggest applicants' claimed invention of forming an oxide on an inner wall as part of the process needed to make applicants' claimed invention. The mere fact that Gardner has to remove an oxide material from the inner walls (that was at best over spray for coating a substrate 401) of the a chamber after the formation a device does not lead one of ordinary skill in the art to make a device by forming an oxide film on the inner walls of a CVD chamber before applicants' device is made.

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being formed on "an inner wall of the processing chamber for forming the top gate type TFT". Gardner et al still further fails to teach or suggest the order in which applicants' claimed method steps are presented. In particular, "forming an oxide on an inner wall of a CVD processing chamber" is performed prior to "doping the source and drain electrodes with p". Again, Gardner et al teaches away from applicants' claimed method by "removing any native oxide" before a layer is formed, see step 304 in Figure 3, column 4, lines 42 - 46 and column 5, lines 16 - 20. Accordingly, it is believed that Ohnuma et al. cannot make obvious applicants' claimed invention, either singularly or in combination with Gardner et al under 35 U.S.C. § 103(a). Furthermore, there is no motivation or suggestions for one skilled in the art to combine the teachings of Ohnuma et al. and Gardner et al as defined in claims 1 - 16. Again, if one were to use the teachings of Gardner et al, one would remove the oxide from Ohnuma et al. However, since Ohnuma et al does not have an oxide film to remove, as claimed in applicants' claims, Gardner et al adds nothing to the Ohnuma et al reference.

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In the event that this response does not result in allowance of all such claims, the undersigned respectfully requests a telephone interview at the Examiner's earliest convenience.

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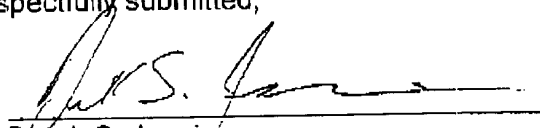


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Applicants request entry of this paper so as to place the file history of this patent application in better form for appeal.

Respectfully submitted,

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